WHAT IS CLAIMED IS:

1. A method of designing an integrated circuit, comprising executing a placement algorithm to place a set of objects within the integrated circuit, wherein the set of objects includes latched objects and non-latched objects and wherein the algorithm places objects to minimize clock signal delay subject to a constraint on the placement distribution of the latched objects relative to the placement distribution of the non-latched objects.

2. The method of claim 1, wherein the latched object and non-latched object placement constraints limit the difference between the latched object center of mass and a non-latched object center of mass, wherein the latched object center of mass equals a sum of size-location products for each latched object divided by the sum of sizes for each latched object.

3. The method of claim 2, wherein the constraints require that the latched object center of mass and the non-latched center of mass both equal the center of mass for all objects.

4. The method of claim 1, wherein the algorithm minimizes clock signal delay by minimizing, subject to the placement constraint, a weighted sum of lengths of interconnects required to connect the objects as placed.

5. The method of claim 4, further comprising performing an unconstrained initial placement algorithm to place the latched and non-latched objects to minimize the sum of interconnect lengths.

6. The method of claim 5, further comprising

synthesizing a clock tree for the objects as placed and for determining signal skew associated with the clock tree; and

invoking the placement algorithm responsive to the determined signal skew exceeding a threshold value.

7. A computer program product for designing an integrated circuit, the program product being stored on a computer readable medium, comprising code means for performing a placement algorithm to place a set of objects within the integrated circuit, wherein the set of objects includes latched objects and non-latched objects and wherein the algorithm places objects to minimize clock signal delay subject to a constraint on latched object placement limiting the extent of latched placement asymmetry.

8. The computer program product of claim 7, wherein the algorithm places objects further to subject to an additional constraint on non-latched object placement limiting the extent of non-latched placement asymmetry.

9. The computer program product of claim 8, wherein the latched object and non-latched object placement constraints limit the difference between the latched object center of mass and a non-latched object center of mass, wherein the latched object center of mass equals a sum of size-location products for each latched object divided by the sum of sizes for each latched object.

10. The computer program product of claim 9, wherein the constraints require that the latched object center of mass and the non-latched center of mass both equal the center of mass for all objects.

11. The computer program product of claim A, wherein the algorithm minimizes clock signal delay by minimizing, subject to the placement constraint, a weighted sum of lengths of interconnects required to connect the objects as placed.

12. The computer program product of claim 11, further comprising:

code means for performing an unconstrained initial placement algorithm to place the latched and non-latched objects to minimize the sum of interconnect lengths;

13. The computer program product of claim 12, further comprising:

code means for synthesizing a clock tree for the objects as placed and for determining signal skew associated with the clock tree; and

code means for invoking the placement algorithm responsive to the determined signal skew exceeding a threshold value.

14. A system for designing an integrated circuit, comprising means for executing a placement algorithm to place a set of objects within the integrated circuit, wherein the set of objects includes latched objects and non-latched objects and wherein the algorithm places objects to minimize clock signal delay subject to a constraint on the placement distribution of the latched objects relative to the placement distribution of the non-latched objects.

15. The system of claim 14, wherein the latched object and non-latched object placement constraints limit the difference between the latched object center of mass and a non-latched object center of mass, wherein the latched object center of mass equals a sum of size-location products for each latched object divided by the sum of sizes for each latched object.

16. The system of claim 15, wherein the constraints require that the latched object center of mass and the non-latched center of mass both equal the center of mass for all objects.

17. The system of claim 1, wherein the algorithm minimizes clock signal delay by minimizing, subject to the placement constraint, a weighted sum of lengths of interconnects required to connect the objects as placed.

18. The system of claim 17, further comprising means for performing an unconstrained initial placement algorithm to place the latched and non-latched objects to minimize the sum of interconnect lengths.

19. The system of claim 18, further comprising

means for synthesizing a clock tree for the objects as placed and for determining signal skew associated with the clock tree; and

means for invoking the placement algorithm responsive to the determined signal skew exceeding a threshold value.

20. The system of claim 14, wherein the constraint on the placement distribution of the latched objects is further characterized as a constraint on the x-axis placement distribution and the y-axis placement distribution of latched objects relative to the x-axis and y-axis placement distribution of the non-latched objects.